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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/924,301	08/08/2001	Won-Ho Lee	29936/37051	3115

4743 7590 01/26/2007  
MARSHALL, GERSTEIN & BORUN LLP  
233 S. WACKER DRIVE, SUITE 6300  
SEARS TOWER  
CHICAGO, IL 60606

EXAMINER

MULPURI, SAVITRI

ART UNIT	PAPER NUMBER
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2812

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/26/2007	PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

**Office Action Summary**

Application No.

09/924,301

Applicant(s)

LEE, WON-HO

Examiner

Savitri Mulpuri

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☐ Responsive to communication(s) filed on 03 November 2006.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 6-8, 10, 11 and 19-26 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 6-8, 10, 11 and 19-26 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                        | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)    | Paper No(s)/Mail Date. _____  |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____   | 6) <input type="checkbox"/> Other: _____                                    |

## DETAILED ACTION

### *Continued Examination Under 37 CFR 1.114*

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114.

Applicant's submission filed on 11/3/2006 has been entered.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 6-8, 10-11, 19-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al (US 6,380,568) in combination with Ishida et al (6,344,396) and Cunningham et al (US 6,479,362).

Lee et al teaches a method of making CMOS image sensor comprising: providing a semiconductor structure, wherein the semiconductor structure includes an impurity region "660" and a gate electrode "640"; forming a first spacer on a first side wall of the gate electrode, wherein the first spacer "680" is

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overlapped with a portion of the impurity region '660'; forming second spacer '682' on a side wall of the first spacer '680' and forming a third spacer '680' on a second sidewall of the gate electrode and forming fourth spacer 682.

With respect to claims 25 Lee et al teaches carrying an implantation to form P- type impurity region "670" in an N-type impurity region "660" to form photo diode and forming floating diffusion region "10, 503,690" spaced away from the impurity by a predetermined distance (see fig.1,5 and 7 , line col.4, lines 34-40).

With respect to claims 7, 20 Lee et al teaches forming insulator layer and perform blanket etching to form spacers (see col. 4, lines 30-34).

Lee et al do not teach removing the fourth spacer "682".

Ishida et al teaches forming first spacer "'3" and forming a fourth spacer "14" (see fig. 1C); removing the fourth spacer "14", by using photo resist as mask, to form asymmetric CMOS transistors (see fig. 1E and related description); forming a second spacer "20" on a side wall of the first spacer and a third spacer "20" on second sidewall of the gate electrode after removing the fourth spacer "14" (see 1 J). It would have been obvious to one of ordinary skill in the art to remove fourth spacer by using photo resist as mask in the invention of Lee et al to avoid short channel effects due to presence of hot carriers since Lee et al also teaches method of making CMOS transistors s as similar to CMOS transistors in Ishida et al (see col.5, lines 5-38).

With respect to claim 8,11, claim 23 Lee does no teach forming spacers with thermal oxide. Cunningham teaches forming spacer from thermal oxide (see

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col.6, lines 34-45). It would have been obvious to one of ordinary skill in the art to form spacers from thermal oxide because thermal oxide or nitride spacers are dense compared to directly deposited oxide or nitride spacers.

### ***Response to Arguments***

Applicant's arguments filed on 10/6/2006 have been fully considered but they are not persuasive. Applicant argues that the reference taken alone or in combination do not teach or suggest as recited by claim 6 at least forming a first spacer on a first side wall of the gate electrode and a fourth spacer on a second side wall of the gate electrode, wherein the first spacer is overlapped with a portion of an impurity region and removing the fourth spacer by photo resist pattern covering the impurity region and the first spacer. However, Lee et al teaches substantially same process as the process recited in the invention except that removing the fourth spacer by using photo resist as a mask. Ishida et al teaches removing the fourth spacer "14" by using photo resist as a mask pattern (see fig. 1D). The invention of Lee et al, as modified by the teaching of Ishida et al, would remove the fourth spacer "680" using photo resist as a mask for avoiding short channel effects.

### ***Conclusion***

.Any inquiry concerning this communication or earlier communications from the examiner should be directed to Savitri Mulpuri whose telephone number

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is 571-272-1677. The examiner can normally be reached on Mon-Fri from 8 a.m. to 4.30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt, can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Savitri Mulpuri  
Primary Examiner  
Art Unit 2812